TEXAS INSTRUMENTS

DAC7573, DAC6573, and DAC5573 Evaluation Module

User's Guide

January 2004

Data Acquisition

SLAU125

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V - V_{DD} +0.3 V and the output voltage range of ±4.5 V and ±18 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the DAC7573, DAC6573, DAC5573 Evaluation Module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

Chapter 1 – EVM Overview

Chapter 2 – PCB Design

Chapter 3 – EVM Operation

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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Data Sheets:	**Literature Number:**
DAC7573	SLAS398
DAC6573	SLAS402
DAC5573	SLAS401
REF02	SBVS-003A
OPA627	PDS-998H
OPA2132	PDS-1309B

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Chapter 1

EVM Overview

This chapter gives a general overview of the DAC7573, DAC6573, and DAC5573 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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1.1 Features

This EVM features the DAC7573, DAC6573 and DAC5573 family of digital-to-analog converters. In this user's guide, the EVM is referred to as the DACx573 EVM to cover all supported DAC parts. The DACx573 EVM provides a quick and easy way to evaluate the functionality and performance of these 12-bit, 10-bit, and 8-bit resolution, quad-channel, and serial I^2C-input DACs. The following table shows the three DAC types this EVM supports. The EVM also provides an I^2C serial interface to communicate with any host microprocessor- or TI DSP-based system.

Table 1-1. Featured DAC Selections

EVM Version	Installed Device (DUT)	DAC Channels	Resolution
DAC7573 EVM	DAC7573IPW	4	12-Bit
DAC6573 EVM	DAC6573IPW	4	10-Bit
DAC5573 EVM	DAC5573IPW	4	8-Bit

1.2 Power Requirements

This section describes the power requirements of this EVM.

1.2.1 Supply Voltage

The power supply requirement for the digital section (V_{DD}) of this EVM is typically 5 V, connected via J5-1 or J6-10 when used with another EVM or interface card. It is referenced to ground through the J5-2 and J6-5 terminals. The power supply requirements for the analog section of this EVM are as follows:

V_{CC} and V_{SS} range from 15.75 V to -15.75 V maximum, and connects through J1-3 and J1-1 respectively, or through the J6-1 and J6-2 terminals.

The 5-VA supply connects through J5-3 or J6-3 and the 3.3-VA supply connects through J6-8.

All analog power supplies are referenced to analog ground through the J1-2 and J6-6 terminals.

The analog power supply for the device under test (DUT), U1, can be supplied by either 5 VA or 3.3 VA via jumper W1. This allows the DACx573 analog section to operate from either supply while the I/O and digital section is powered by 5 V, V_{DD}.

The V_{CC} supply is mainly used as the positive rail of the external output operational amplifier (op amp), U2, the reference chip, U3, and the reference buffer, U8. The negative rail of the output op amp, U2, can be selected between V_{SS} and AGND via jumper W5. The external op amp is installed as an option to provide output signal conditioning, to boost capacitive load drive (via W15), and for other output-mode requirements.

Caution

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The 5-V precision voltage reference is provided to supply the external voltage reference for the DAC through REF02, U3, via jumper W4 by shorting pins 1 and 2. The reference voltage goes through 100-kΩ potentiometer R11 in series with 20-kΩ R10 to allow the user to adjust the reference voltage to a desired level. The voltage reference is then buffered through U8A to the DUT. Test points TP1, TP2, and TP5 are also provided, as well as J4-18 and J4-20, to allow the user to connect another external reference source if the onboard reference circuit is not used. The external voltage reference must not exceed 5 Vdc.

The REF02 precision reference is powered by V_{CC} (15 V) through the J1-3 or J6-1 terminal.

Caution

When applying an external voltage reference through TP1 or J4-20, make sure that it does not exceed 5 V maximum. Otherwise, this can permanently damage the installed device under test (DUT).

1.3 EVM Basic Functions

The DACx573 EVM is a functional-evaluation platform to demonstrate the operation of the DACx573 family of digital-to-analog converters. Functional evaluation of the DAC device can be conducted with any microprocessor, TI DSP, or a waveform generator.

Header connectors J2 and P2 allow control signals and data from a host processor or waveform generator to interface with the DACx573 EVM using a custom-built cable.

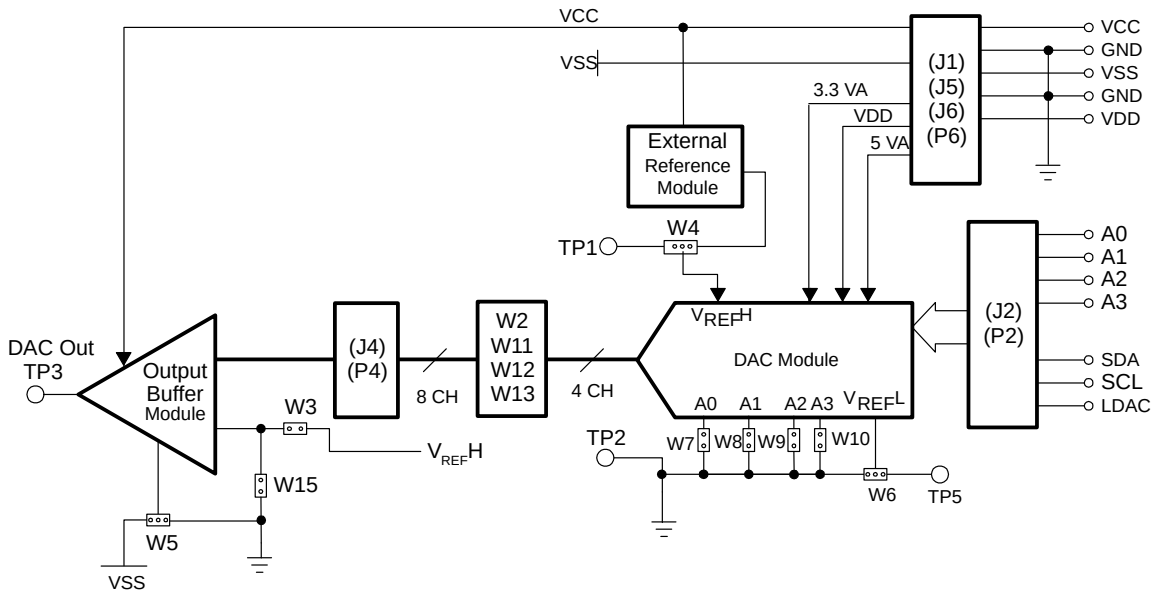
Specific adapter interface boards are also available for many TI DSP Starter Kits (DSKs). Specify the correct adapter interface board for the TI DSP Starter Kit to be used. In addition, an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor is available that directly interfaces with this EVM. For more information regarding the adapter-interface board or the HPA449 platform, please call Texas Instruments or send email to dataconvapps@list.ti.com.

The DAC outputs can be monitored through the J4 header connector. All the outputs can be switched by their respective jumpers W2, W11, W12, and W13 for stacking. Stacking allows eight DAC channels to be used, provided that the I^2C address is unique for each EVM board stacked.

In addition, one DAC output can be fed to the noninverting side of output op amp U2 by installing a jumper across the appropriate pins of J4. Output op amp U2 must first be configured correctly for the desired waveform characteristic. Refer to Chapter 3 of this user's guide for more information.

A block diagram of the EVM is shown in Figure 1-1.

Figure 1-1. EVM Block Diagram



Chapter 2

PCB Design

This chapter describes the physical and mechanical characteristics of the EVM. The bill of materials is also included in this chapter.

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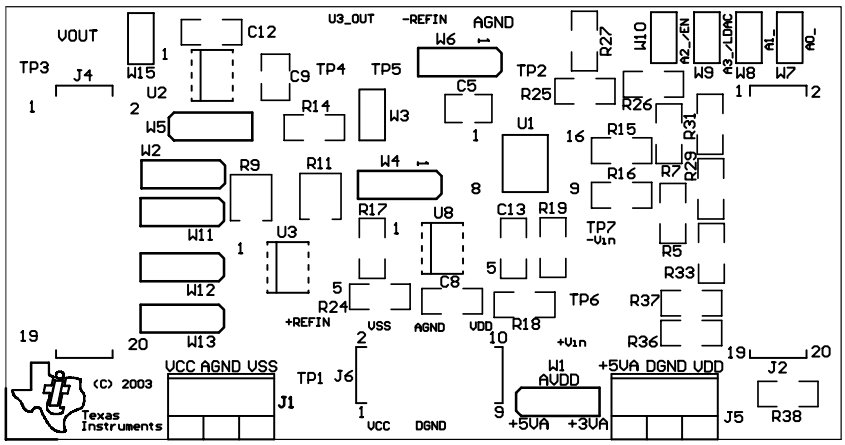
2.1 PCB Layout

The DACx573 EVM demonstrates the performance of the installed DAC device under test, as specified in the data sheet. Careful analysis of the physical restrictions and performance-degrading factors of the EVM is vital to a successful design implementation. The obvious attributes that can cause poor performance of the EVM can be avoided during schematic design by proper component selection and correct circuit-design practices. The circuit must include adequate bypassing, identifying, and managing the analog and digital signals and understanding the mechanical attributes of the components.

The less obvious part of the design lies in the PCB layout. The main concerns are component placement and proper signal routing. The bypass capacitors must be placed as close as possible to the pins and the analog and digital signals must be properly separated from each other. The power and ground planes are very important and require careful consideration. A solid plane is preferred, but sometimes impractical. When solid planes are not possible, a well-designed split plane can suffice. When considering a split-plane design, analyze the component placement and carefully divide the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling noise and other effects that can contribute to DAC output error. To ensure that return currents are handled properly, route the appropriate signals only in their respective sections. Route analog traces only directly above or below the analog section, and the digital traces in the digital section. Minimize trace length, but use the widest possible trace allowable in the design. These design practices are demonstrated in subsequent figures in this section.

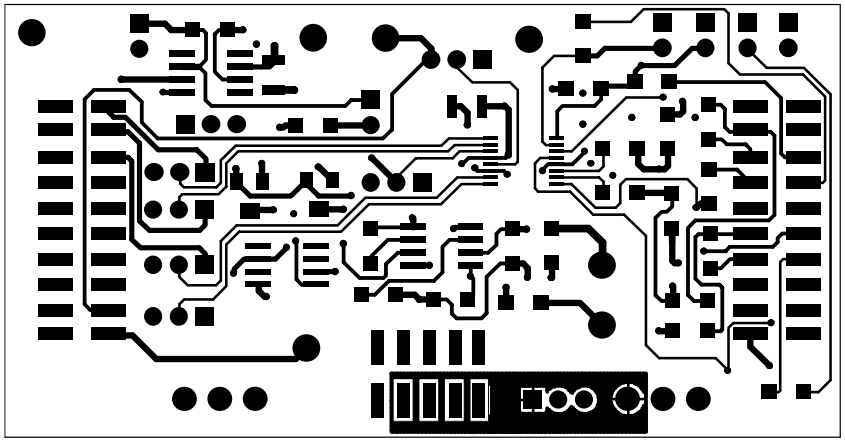
The DACx573 EVM board is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has a dimension of 43,1800 mm (1.7000 inch) X 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2-1 through Figure 2-6 show the individual artwork layers.

Figure 2-1. Top Silkscreen



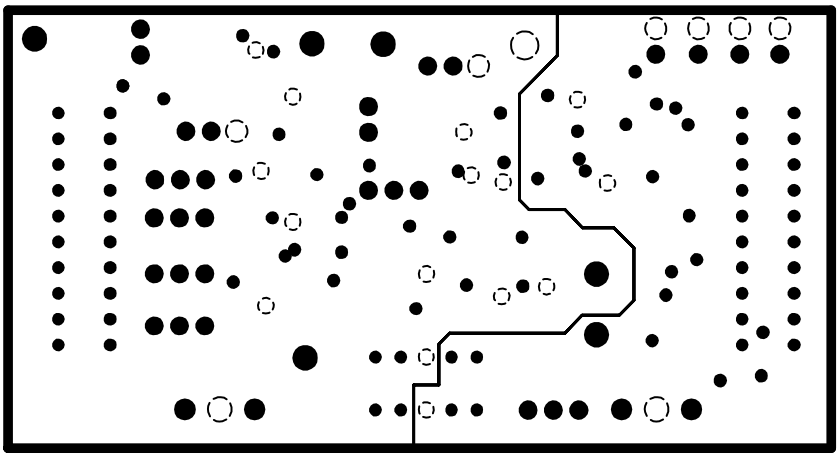
DACx573 REV A LAYER SILKSCREEN TOP

Figure 2-2. Layer 1 (Top Signal Plane)



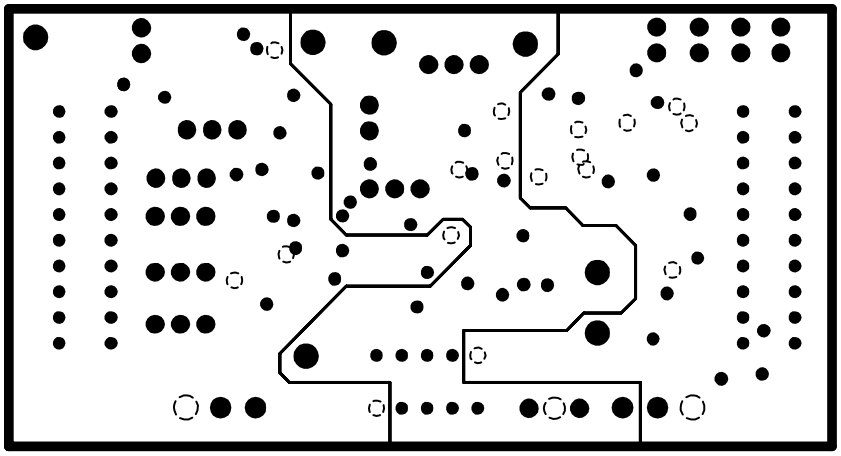
DACx573 REV A LAYER 1 TOP SIGNAL LAYER

Figure 2-3. Layer 2 (Ground Plane)



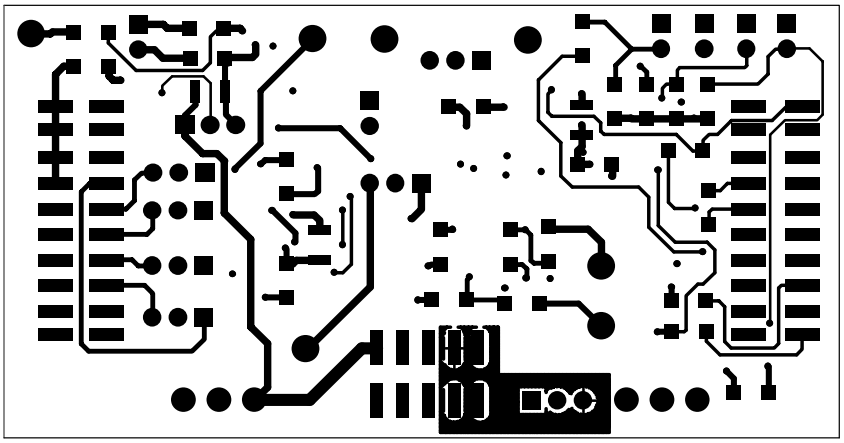
DACx573 REV A LAYER 2 SPLIT GND PLANE

Figure 2-4. Layer 3 (Power Plane)



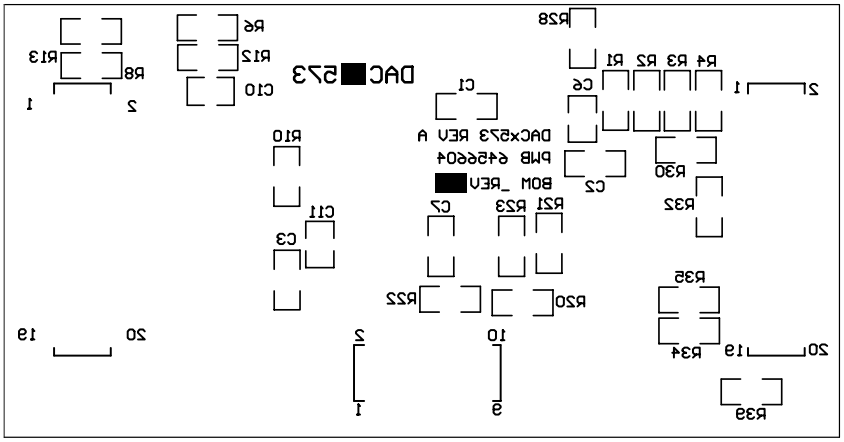
DACx5/3 REV A LAYER 3 SPLIT POWER PLANE

Figure 2-5. Layer 4 (Bottom Signal Plane)



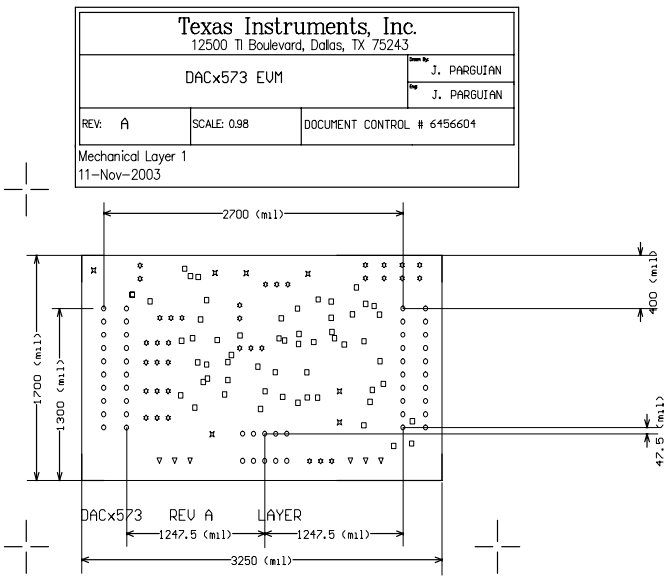
DACx573 REV A LAYER 4 BOTTOM SIGNAL LAYER

Figure 2-6. Bottom Silkscreen



DACx573 REV A LAYER SILKSCREEN BOTTOM

Figure 2-7. Drill Drawing



Notes:

1. PWB TO BE FABRICATED TO MEET OR EXCEED IPC-6012, CLASS 3 STANDARDS AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 3 - CURRENT REVISIONS
2. BOARD MATERIAL AND CONSTRUCTION TO BE UL APPROVED AND MARKED ON THE FINISHED BOARD.
3. LAMINATE MATERIAL: COPPER-CLAD FR-4
4. COPPER WEIGHT: 1oz FINISHED
5. FINISHED THICKNESS: .062 +/- .010
6. MIN PLATING THICKNESS IN THROUGH HOLES: .001"
7. SMOBC / HASL
8. LPI SOLDERMASK BOTH SIDES USING APPROPRIATE LAYER ARTWORK: COLOR = GREEN
9. LPI SILKSCREEN AS REQUIRED: COLOR - WHITE
10. VENDER INFORMATION TO BE INCORPORATED ON BACK SIDE WHENEVER POSSIBLE
11. MINIMUM COPPER CONDUCTOR WIDTH IS: 10 MILS MINIMUM CONDUCTOR SPACING IS: 8 MILS
12. NUMBER OF FINISHED LAYERS: 4

○	50	13mil	0.3302mm	PTH
□	58	15mil	0.381mm	PTH
◇	36	37mil	0.9398mm	PTH
▽	6	47.244mil	1.2mm	PTH
⌘	7	62mil	1.5748mm	PTH
	157	Total		

2.2 Bill of Materials

Table 2-1. Parts List

Item #	Qty	Designator	Mfr.	Part Number	Description
1	2	C9 C10	Panasonic	ECUV1H105JCH	1-µF, 1206 multilayer-ceramic capacitor
2	4	C1 C2 C3 C7	Panasonic	ECJ3VB1C104K	0.1-µF, 1206 multilayer-ceramic capacitor
3	1	C12	Panasonic	ECUV1H102JCH	1-nF, 1206 multilayer ceramic capacitor
4	3	C5 C6 C11	Kemet	C1210C106K8PAC	10-µF, 1210 multilayer ceramic X5R capacitor
5	17	R8 R17 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39	Panasonic	ERJ-8GEY0R00V	0-Ω, 1/4-W 1206 chip resistor
6	2	R15 R16	Panasonic	ERJ-8GEYJ431V	430-Ω, 1/4-W 1206 chip resistor
7	1	R13	Panasonic	ERJ-8GEYJ101V	100-Ω,1/4-W 1206 chip resistor
8	1	R10	Panasonic	ERJ-8ENF2002V	20-kΩ,1/4-W 1206 chip resistor
9	6	R1 R2 R3 R4 R5 R7	Panasonic	ERJ-8GEYJ302V	3-kΩ, 1/4-W 1206 chip resistor
10	3	R6 R12 R14	Panasonic	ERJ-8ENF1002V	10-kΩ,, 1/4-W 1206 chip resistor
11	1	R9	Bourns	3214W-203E	20-kΩ, BOURNS_32X4W series 5T pot
12	1	R11	Bourns	3214W-104E	100-kΩ, BOURNS_32X4W series 5T pot
13	1	J6	Samtec	TSM-105-01-T-DV	5X2X0.1, 10-pin 3 A isolated power socket
14	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10X2X.1, 20 Pin 0.025” sq SMT socket
15	2	J1 J5	On-Shore Technology	ED555/3DS	3-pin terminal connector
16	1	U1	Texas Instruments	DAC7573IPW	12-bit, quad output, I^2C DAC
				DAC6573IPW	10-bit, quad output, I^2C DAC
				DAC5573IPW	8-bit, quad output, I^2C DAC
17	1	U2	Texas Instruments	OPA627AU	8-SOP(D) precision op amp
18	1	U3	Texas Instruments	REF02AU	5-V, 8-SOP(D) precision voltage reference
19	1	U8	Texas Instruments	OPA2132UA	8-SOP(D) Dual Precision Op Amp
20	7	TP1 TP2 TP3 TP4 TP5 TP6 TP7	Mill-max	2348-2-01-00-00-07-0	Turret terminal test point
21	2	P2 P4 (see Note)	Samtec	SSW-110-22-S-D-VS-P	20-pin 0.025” square SMT terminal strips
22	1	P6 (see Note)	Samtec	SSW-105-F-D-VS-K	3-A isolated 10-pin power header
23	6	W3 W7 W8 W9 W10 W15	Molex	22-03-2021	2 position jumper, 0.1” spacing
24	8	W1 W2 W4 W5 W6 W11 W12 W13	Molex	22-03-2031	3 position jumper, 0.1” spacing

Note: P2, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed on the bottom side of the PC board opposite the J-designated counterpart. Example, J2 is installed on the top side while P2 is installed in the bottom side opposite of J2. Not all parts listed in the BOM are installed in the EVM as they are specific to the DUT installed.

Chapter 3

EVM Operation

This chapter details the operation of the EVM to guide the user in evaluating the onboard DAC and in interfacing the EVM to a host processor.

Refer to the specific DAC data sheet, as listed in the *Related Documentation From Texas Instruments* section in the *Preface* of this user's guide for more information about the DAC serial interface and other related topics.

The EVM board is factory-configured to operate in the unipolar output mode.

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3.1 Factory Default Setting

The EVM board is factory-configured to operate in unipolar 5-V output mode.

Table 3-1. DACx573EVM Factory-Default Jumper Configuration

DACx573 EVM CONFIGURATION		
Reference	**Jumper Position**	**Function**
W1	1-2	Analog supply for the DACx573 is 5 VA.
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	Open	$V_{REF}H$ is not routed to the inverting input of the op amp.
W4	1-2	Onboard external buffered reference U3 is routed to $V_{REF}H$.
W5	1-2	Negative supply rail of U2 op amp is supplied by V_{SS}.
W6	1-2	$V_{REF}L$ is tied to AGND.
W7	Closed	A0 pin is tied to DGND.
W8	Closed	A1 pin is tied to DGND.
W9	Closed	A3 pin is tied to DGND.
W10	Closed	A2 pin is tied to DGND.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
W15	Closed	Output op amp U2 is configured for a gain of 2.
J4	1-2	DAC output A ($V_{OUT}A$) is connected to the noninverting input of output op amp U2.

3.2 Host Processor Interface

Because the host processor controls the DAC, proper operation depends on the correct interface of the host processor and the EVM board. Properly written code is also required to operate the DAC.

A host-platform-specific cable assembly can be made to connect the EVM to the host processor through J2 for the I^2C serial control and data signals. The output is monitored through J4.

An interface adapter board is available for specific TI DSP starter kits as well as for an MSP430-based microprocessor as mentioned in section 1.3. Using the interface board alleviates the tedious task of building custom cables and allows easy configuration of a simple evaluation system.

This DACx573 EVM interfaces with any host processor capable of I^2C protocols or the popular TI DSP. For more information regarding the serial interface of the particular DAC installed, refer to the specific DAC data sheet, as listed in the *Related Documentation From Texas Instruments* section in the *Preface* of this user's guide.

3.3 EVM Stacking

EVM stacking enables the designer to evaluate two DACx573s in tandem to yield an eight-channel output. A maximum of two DACx573 EVMs are allowed because the output terminal, J4, dictates the number of DAC channels that can be connected without colliding. Table 3-2 shows how the DAC output channels are mapped to the output terminal, J4, with respect to the jumper positions of W2, W11, W12, and W13.

Table 3-2. DACx573 Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
	2-3	DAC output A ($V_{OUT}A$) is routed to J4-10.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
	2-3	DAC output B ($V_{OUT}B$) is routed to J4-12.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
	2-3	DAC output C ($V_{OUT}C$) is routed to J4-14.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
	2-3	DAC output D ($V_{OUT}D$) is routed to J4-16.

Each DAC EVM in a stacked configuration must have a unique I^2C address. This is accomplished by configuring address jumpers W7 and W8 (refer to the data sheet for I^2C addressing).

The LDAC signal can be shared to have a synchronous DAC-output update and can be hardware-driven by GPIO0. If software control of the LDAC is desired, the GPIO0 signal must be set low through software or J2-pin 2 can be strapped to DGND.

3.4 Output Op Amp

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time because the odd numbered pins (J4-1 to J4-7) are tied together. The output op amp gain is configured at two by default. The unbuffered outputs of the DAC can be probed through the even pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into an interface board. J4 also provides easy access for monitoring up to eight DAC channels when stacking two EVMs together, as described in section 3.3.

The following sections describe various configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC. However, it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match the desired wave shape by simply removing R7 and C11 and replacing them with the desired values. R7 can be replaced with a zero-ohm resistor and C11 can be left open, if desired.

Table 3-3 shows the jumper settings for the unity gain configuration of the output buffer in unipolar or bipolar supply mode.

Table 3-3. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Open	Open	Disconnects TP2 input or AGND from the inverting input of the op amp
W5	2-3	1-2	Supplies V_{SS} to the negative rail of the op amp or ties it to AGND
W15	Open	Open	Disconnects negative input of the op amp from AGND

3.4.2 Output Gain of Two

Table 3-4 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 3-4. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Closed	Closed	Inverting input of output op amp U2 is connected to $V_{REF}H$ for use as its offset voltage with a gain of 2. Jumper W15 must be open.
	Open	Open	$V_{REF}H$ is disconnected from the inverting input of output op amp U2. Jumper W15 must be closed.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op amp U2 for bipolar supply mode, or ties it to AGND for unipolar supply mode
W15	Closed	Closed	Configures op amp U2 for a gain of 2 output without an offset voltage. Jumper W3 must be open.
	Open	Open	Inverting input of op amp U2 is disconnected from AGND. Jumper W3 must be closed.

3.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive loads. All op amps under certain conditions may become unstable depending on configuration, gain, and load value. In unity gain, the OPA627 op amp performs well with large capacitive loads. Increasing the gain and adding a load resistor further improves the capacitive load drive capability.

Table 3-5 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 3-5. Capacitive-Load Drive Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Open	Open	$V_{REF}H$ is disconnected from the inverting input of output op amp U2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op amp U2 for bipolar supply, or ties it to AGND for unipolar supply.
W15	Open	Open	Capacitive load drive output of DAC is routed to jumper-W15 pin 1, and this pin can be used as the output terminal.

3.4.4 Optional Signal Conditioning Op Amp (U8B)

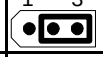
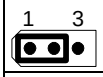
One device of the dual-op amp OPA2132 (U8) is used for reference buffering (U8A), while the other is unused. This unused op amp (U8B) is available for user-configured circuitry. The 1206-package resistor and capacitor footprints associated with the U8B op amp are unpopulated and available for easy configuration. TP6 and TP7 test points are not installed for maximum flexibility of input-signal configuration. No test point is available for the output due to space restrictions, but a wire can be simply soldered to the output of the op amp via the unused component pads connected to it.

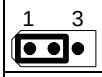
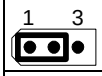
Once the op amp circuit design is determined, it is easily implemented by simply populating the desired components and leaving unused component footprints unpopulated.

3.5 Jumper Setting

Table 3-6 shows the function of each specific jumper setting of the EVM.

Table 3-6. Jumper Setting Function

Reference	Jumper Setting	Function
W1		5-V analog supply is selected for AV_{DD}.
		+3.3-V analog supply is selected for AV_{DD}.
W2		Routes $V_{OUT}A$ to J4-2
		Routes $V_{OUT}A$ to J4-10
W3		Disconnects $V_{REF}H$ to the inverting input of output op amp U2.
		Connects $V_{REF}H$ to the inverting input of output op amp U2.
W4		Routes the adjustable, buffered, onboard 5-V reference to the $V_{REF}H$ input of the DACx573.
		Routes the user supplied reference from TP1 or J4-20 to the $V_{REF}H$ input of the DACx573.
W5		Negative supply rail of the output op amp U2 is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output op amp U2 is tied to AGND for unipolar operation.
W6		$V_{REF}L$ is tied to AGND.
		Routes the user-supplied negative reference from TP2 or J4-18 to the $V_{REF}L$ input of the DACx573. This voltage must be within the range of 0V to $V_{REF}H$.
W7		A0 is set high through pullup-resistor R4. A0 can be driven by GPIO5.
		A0 is set low.
W8		A1 is set high through pullup-resistor R3. A1 can be driven by GPIO4.
		A1 is set low.
W9		A3 is set high through pullup-resistor R2. A3 can be driven by GPIO1.
		LDAC pin is set low and DAC update is accomplished via software.
W10		A2 is set high through pullup-resistor R1. A2 can be driven by GPIO3.
		A2 pin is set low.
W11		Routes $V_{OUT}B$ to J4-4
		Routes $V_{OUT}B$ to J4-12

Reference	Jumper Setting	Function
W12		Routes $V_{OUT}C$ to J4-6
		Routes $V_{OUT}C$ to J4-14
W13		Routes $V_{OUT}D$ to J4-8
		Routes $V_{OUT}D$ to J4-16
W15		Disconnects the inverting input of output op amp U2 from AGND.
		Connects the inverting input of output op amp U2 to AGND for gain of 2.

Legend:  Indicates the corresponding pins that are shorted or closed.

3.6 Schematic

The schematic is on the following page.

Revision History		
REV	ECN Number	Approved

DAC7573 = 12-Bit
DAC6573 = 10-Bit
DAC5573 = 8-Bit

NOTE: Voltage range of -REFin input should not exceed 0 - VrefH.

VCC = +15V Analog
VDD = +2.7V to +5.0V Digital
VSS = 0V to -15V Analog

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DACx573 EVM			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6456605		REV: A
Drawn By:	DATE: 1-Dec-2003	SIZE:	SHEET: OF: 1
FILE: DAC7573 RevA.Sch			